CLAIMS

What is claimed is:

1. A method of optimizing a bond out design comprising steps of:

(a) receiving as input an initial bond out design including at least one selected I/O pad and a top redistribution layer;

(b) determining whether to include a lower redistribution layer in an optimized bond out design;

(c) selecting a trace design to be included in the optimized bond out design for connecting the selected I/O pad to the top redistribution layer according to a bump function of the selected I/O pad; and

(d) generating as output the optimized bond out design.

2. The method of Claim 1 wherein step (b) comprises including a lower redistribution layer in the optimized bond out design.

3. The method of Claim 2 wherein step (b) further comprises placing a plurality of inner vias to be included in the optimized bond out design between the selected I/O pad and the lower redistribution layer to connect the selected I/O pad to the lower redistribution layer.

4. The method of Claim 3 further comprising placing the plurality of inner vias to be included in the optimized bond out design within a projection of a passivation opening of the selected I/O pad onto the lower redistribution layer.

5. The method of Claim 4 further comprising distributing the plurality of inner vias in the optimized bond out design to minimize peak current density in the selected I/O pad.

6. The method of Claim 4 further comprising extending trace metal in the optimized bond out design into the projection of the passivation opening by at least one-third of a width of the projection of the passivation opening.

7. The method of Claim 4 further comprising arranging the plurality of inner vias to be included in the optimized bond out design in a staggered pattern to distribute current evenly across the passivation opening.

8. The method of Claim 7 further comprising shortening trace metal in the lower redistribution layer to allow routing of traces in the lower redistribution layer underneath the selected I/O pad.

9. The method of Claim 8 further comprising arranging the inner plurality of vias in the optimized bond out design within an area equal to about two-thirds of a width of the passivation opening to allow additional routing of traces underneath the selected I/O pad.

10. The method of Claim 1 further comprising a step of placing a plurality of outer vias to be included in the optimized bond out design between the top redistribution layer and the lower redistribution layer to balance current between the top redistribution layer and the lower redistribution layer.

11. The method of Claim 1 wherein step (d) comprises selecting one of a full-width trace and a tapered trace.

12. The method of Claim 1 wherein step (c) includes determining whether to include a lower redistribution layer as a function of the design maximum bump current value or as a function of a metal layer packaging technology.

13. A computer program product for optimizing a bond out design comprising:

a medium for embodying a computer program for input to a computer; and

a computer program embodied in the medium for causing the computer to perform steps of:

(a) receiving as input an initial bond out design including at least one selected I/O pad and a top redistribution layer;

(b) determining whether to include a lower redistribution layer in an optimized bond out design;

(c) selecting a trace design to be included in the optimized bond out design for connecting the selected I/O pad to the top redistribution layer according to a bump function of the selected I/O pad; and

(d) generating as output the optimized bond out design.

14. The computer program product of Claim 13 wherein step (b) comprises including a lower redistribution layer in the optimized bond out design.

15. The computer program product of Claim 14 wherein step (b) further comprises placing a plurality of inner vias in the optimized bond out design between the selected I/O pad and the lower redistribution layer to connect the selected I/O pad to the lower redistribution layer.

16. The computer program product of Claim 15 further comprising placing the plurality of inner vias in the optimized bond out design within a projection of a

passivation opening of the selected I/O pad onto the lower redistribution layer.

17. The computer program product of Claim 16 further comprising distributing the plurality of inner vias in the optimized bond out design to minimize peak current density in the selected I/O pad.

18. The computer program product of Claim 17 further comprising extending trace metal in the optimized bond out design into the projection of the passivation opening by at least one-third of a width of the projection of the passivation opening.

19. The computer program product of Claim 18 further comprising arranging the plurality of inner vias to be included in the optimized bond out design in a staggered pattern to distribute current evenly across the passivation opening.

20. The computer program product of Claim 19 further comprising shortening trace metal in the lower redistribution layer to allow routing of traces underneath the selected I/O pad.

21. The computer program product of Claim 20 further comprising arranging the inner plurality of vias to be included in the optimized bond out design within an

area equal to about two-thirds of a width of the passivation opening to allow additional routing of traces underneath the selected I/O pad.

22. The computer program product of Claim 13 further comprising placing a plurality of outer vias in the optimized bond out design between the top redistribution layer and the lower redistribution layer to balance current between the top redistribution layer and the lower redistribution layer.

23. The computer program product of Claim 13 wherein step (d) comprises selecting one of a full-width trace width and a tapered trace.

24. The computer program product of Claim 13 wherein step (c) includes determining whether to include a lower redistribution layer as one of a function of the design maximum bump current value and a function of a metal layer packaging technology.

25. A method of optimizing a bond out design comprising steps of:

(a) receiving as input an initial bond out design including at least one selected I/O pad and a top redistribution layer;

(b) if a lower redistribution layer is to be included in an optimized bond out design, then

transferring control to (g), else transferring control to (c);

(c) if a bump function of the selected I/O pad is for a power or ground connection, then transferring control to step (d), else transferring control to step (e);

(d) selecting a full-width trace to be included in the optimized bond out design for connecting the top redistribution layer to the selected I/O pad and transferring control to step (u);

(e) if a full-width trace is allowed for the selected I/O pad, then transferring control to step (d), else transferring control to step (f);

(f) selecting a tapered trace to be included in the optimized bond out design for connecting the top redistribution layer to the selected I/O pad and transferring control to step (u);

(g) including a lower redistribution layer in the optimized bond out design;

(h) if the bump function of the selected I/O pad is for a power or ground connection, then transferring control to step (i), else transferring control to step (n);

(i) if there are no traces routed underneath the selected I/O pad, then transferring control to step (j), else transferring control to step (l);

(j) connecting the top redistribution layer to the lower redistribution layer in the optimized bond out

design by a plurality of inner vias distributed within the projection of the passivation opening onto the lower redistribution layer and by a plurality of outer vias to distribute current evenly between the top redistribution layer and the lower redistribution layer;

(k) selecting a full-width trace to be included in the optimized bond out design for connecting the top redistribution layer to the selected I/O pad and transferring control to step (u);

(l) selecting a full-width trace to be included in the optimized bond out design for connecting the top redistribution layer to the selected I/O pad;

(m) connecting the top redistribution layer to the lower redistribution layer in the optimized bond out design by at least one inner via placed within the projection of the passivation opening onto the lower redistribution layer and by at least one outer via to distribute current evenly between the top redistribution layer and the lower redistribution layer and transferring control to step (u);

(n) if there are no traces routed underneath the selected I/O pad, then transferring control to step (o), else transferring control to step (q);

(o) selecting a full-width trace to be included in the optimized bond out design for connecting the top redistribution layer to the selected I/O pad;

(p) connecting the top redistribution layer to the lower redistribution layer in the optimized bond out

design by a plurality of inner vias distributed within the projection of the passivation opening onto the lower redistribution layer and by a plurality of outer vias to distribute current evenly between the top redistribution layer and the lower redistribution layer and transferring control to step (u);

(q) if a full width trace is possible for the selected I/O pad, then transferring control to step (r), else transferring control to step (s),

(r) selecting a full-width trace in the optimized bond out design for connecting the top redistribution layer to the selected I/O pad and transferring control to step (t);

(s) selecting a tapered trace to be included in the optimized bond out design for connecting the top redistribution layer to the selected I/O pad;

(t) connecting the top redistribution layer to the lower redistribution layer in the optimized bond out design by at least one inner via placed within the projection of the passivation opening onto the lower redistribution layer and by at least one outer via to distribute current evenly between the top redistribution layer and the lower redistribution layer; and

(u) generating as output the optimized bond out design.